

## INFORMATION DISCLOSURE CITATION

Atty. Docket No.	06720.0086-01	Serial No.	TO BE ASSIGNED
Applicant	Chyh-Yih CHANG		
Filing Date	September 25, 2003	Group:	TO BE ASSIGNED

U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
JS		6,258,634	07/10/2001	Wang et al.			
		5,910,874	06/08/1999	Iniewski et al.			
		5,646,808	07/08/1997	Nakayama			
		5,519,242	05/21/1996	Avery			
		5,631,793	05/20/1997	Ker et al.			
		5,811,857	09/22/1998	Assaderaghi et al.			
		5,502,328	03/26/96	Chen et al.			
		5,581,104	12/03/96	Lowrey et al.			
JS		5,990,520	11/23/99	Noorlag et al.			
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
JS	M-D. KER, et al., "CMOS On-Chip ESD Protection Design with Substrate-triggering Technique," Proc. of ICECS, Vol. 1, pp. 273-276, 1998
JS	C. Duvvury et al., "Dynamic Gate Coupling for NMOS for Efficient Output ESD Protection", Proc. of IRPS, pp. 141-150, 1992

Examiner	<i>[Signature]</i>	Date Considered	5-11-5
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	5,932,918	08/03/99	Krakauer			
	6,015,992	01/18/00	Chatterjee et al.			
	5,453,384	09/26/95	Chatterjee			

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	M. Nagata, J. Nagai, K. Hijikata, T. Morie, and A. Iwata, "Physical Design Guides for Substrate Noise Reduction in CMOS Digital Circuits", <i>IEEE Journal of Solid-State Circuits</i> , vol. 36, pp. 539-549, 2001.
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	M.-D. Ker, "Whole-Chip ESD Protection Design with Efficient VDD-to-VSS ESD Clamp Circuit for Submicron CMOS VLSI", <i>IEEE Trans. on Electron Devices</i> , vol. 46, pp. 173-183, 1999

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	5,754,381	05/19/1998	Ker			
	5,465,189	11/07/1995	Polgreen et al.			
	5,225,702	07/06/1993	Chatterjee			
	5,012,317	04/30/1991	Rountre			
28	4,939,616	07/03/1990	Rountree			

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JY	5,629,544	05/13/97	Voldman et al.			
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	5,940,258	08/17/99	Duvvury			
	5,807,791	09/15/98	Bertin et al			
	5,719,737	02/17/98	Maloney			
JY	5,654,862	08/05/97	Worley et al.			

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	G.P. Singh, et al., "High-Voltage-Tolerant I/O Buffers with Low-Voltage CMOS Process," IEEE Journal of Solid-State Circuits, vol.34, no. 11, pp. 1512-1525, Nov. 1999.
JY	H. Sanchez, et al., "A Versatile 3.3/2.5/1.8-V CMOS I/O Driver Built in 02. - $\mu$ m, 3.5-nm Tox, 1.8 -V CMOS Technology, " IEEE Journal of Solid-State Circuits, vol.34 no. 11.pp. 1501-1511, Nov. 1999

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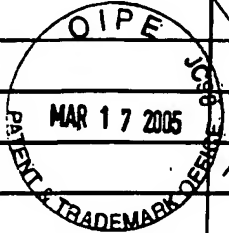
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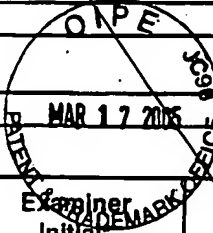
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# INFORMATION DISCLOSURE CITATION

OMB No. 0651-0011

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